LINEAR ASSOCIATIVE MEMORY-BASED HARDWARE ARCHITECTURE FOR FAULT TOLERANT ASIC/FPGA WORK-AROUND

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ABSTRACT OF THE DISCLOSURE

A programmable logic unit (e.g., an ASIC or FPGA) having a feedforward linear associative memory (LAM) neural network checking circuit which classifies input vectors to a faulty hardware block as either good or not good and, when a new input vector is classified as not good, blocks a corresponding output vector of the faulty hardware block, enables a software work-around for the new input vector, and accepts the software work-around input as the output vector of the programmable logic circuit. The feedforward LAM neural network checking circuit has a weight matrix whose elements are based on a set of known bad input vectors for said faulty hardware block. The feedforward LAM neural network checking circuit may update the weight matrix online using one or more additional bad input vectors. A discrete Hopfield algorithm is used to calculate the weight matrix W. The feedforward LAM neural network checking circuit calculates an output vector $a^{(m)}$ by multiplying the weight matrix W by the new input vector $b^{(m)}$, that is, $a^{(m)} = Wb^{(m)}$, adjusts elements of the output vector $a^{(m)}$ by respective thresholds, and processes the elements using a plurality of non-linear units to provide an output of 1 when a given adjusted element is positive, and provide an output of 0 when a given adjusted element is not positive. If a vector constructed of the outputs of these non-linear units matches with an entry in a content-addressable memory (CAM) storing the set of known bad vectors (a CAM hit), then the new input vector is classified as not good.